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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,856	08/23/2002	John Bruno	00100.02.0038 (020038T)	4595
29153	7590 07/19/2005		EXAMINER	
ATI TECHNOLOGIES, INC.			HA, NATHAN W	
	ER PRICE KAUFMAN & ALLE STREET	E KAMMHOLZ, P.C.	ART UNIT	PAPER NUMBER
CHICAGO,			2814	

DATE MAILED: 07/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

1'A		
	Application No.	Applicant(s)
Office Action Summany	10/064,856	BRUNO, JOHN
Office Action Summary	Examiner	Art Unit
The MANUALC DATE of this communication on	Nathan W. Ha	2814
The MAILING DATE of this communication ap Period for Reply	pears on the cover sneet wi	tn tne correspondence address
A SHORTENED STATUTORY PERIOD FOR REPL THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1. after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a rep If NO period for reply is specified above, the maximum statutory period Failure to reply within the set or extended period for reply will, by statut Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	.136(a). In no event, however, may a reply within the statutory minimum of thirts will apply and will expire SIX (6) MON te, cause the application to become AB	eply be timely filed y (30) days will be considered timely. THS from the mailing date of this communication. ANDONED (35 U.S.C. § 133).
Status		
 1) Responsive to communication(s) filed on 20 ft 2a) This action is FINAL. 2b) This action is FINAL. 3) Since this application is in condition for allowed closed in accordance with the practice under 	is action is non-final. ance except for formal matt	•
Disposition of Claims		
4) ☐ Claim(s) 1-16 and 21-23 is/are pending in the 4a) Of the above claim(s) is/are withdra 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-16 and 21-23 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or	awn from consideration.	
Application Papers		
9) The specification is objected to by the Examin 10) The drawing(s) filed on is/are: a) accomposed and applicant may not request that any objection to the Replacement drawing sheet(s) including the correct the oath or declaration is objected to by the Examination.	cepted or b) objected to le drawing(s) be held in abeyan ction is required if the drawing(ce. See 37 CFR 1.85(a). s) is objected to. See 37 CFR 1.121(d).
Priority under 35 U.S.C. § 119		
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority application from the International Bureat* See the attached detailed Office action for a list	nts have been received. nts have been received in A ority documents have been au (PCT Rule 17.2(a)).	pplication No received in this National Stage
Attachment(s)		
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08 Paper No(s)/Mail Date	Paper No(s	ummary (PTO-413))/Mail Date Iformal Patent Application (PTO-152)

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DETAILED ACTION

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 4. Claims 1-2, 5-9, and 21-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Urakawa (US 2003/0015792, previously cited.)

In regard to claims 1 and 21, in fig. 19, Urakawa discloses an integrated circuit comprising:

a standard dimension carrier substrate, or package substrate;

an information router, or logic chip, integrated on the carrier substrate; and system memory, or memory chip operative to store system instructions also integrated on the substrate and in electrical communication with the router via at least one of a plurality of electrical leads directly connected to the carrier substrate, wherein the system instructions may be stored and received from the system memory through the information router.

In regard to claim 2, wherein the information router is disposed an application specific integrated circuit die, fig. 19.

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In regard to claims 5 and 9, wherein the application specific integrated circuit die is coupled to at least one of the plurality of electrical leads associated with the carrier substrate using a plurality of wire bonds. See fig. 19.

In regard to claim 6, wherein the system memory is disposed on a top surface of the carrier substrate and the application specific integrated circuit die is coupled to a bottom surface of the carrier substrate of the packaged chip using a flip chip technology (fig. 21).

In regard to claim 7, wherein the system memory is disposed within a chip scale package memory having a plurality of contact pin, wherein the contact pins are soldered to the carrier substrate (fig. 20b).

Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. Claims 3-4 and 10-16, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urakawa as applied to claims 1-2 and 5-9 above, and further in view of Melo et al. (US 6,243,817, previously cited, hereinafter, Melo.)

In regard to claims 3-4, 10-12, and 22, Urakawa discloses all of the claimed limitations as mentioned above except the substrate includes more devices such graphic chip and a north bridge.

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Melo, in fig. 1, discloses an analogous package and further discloses that the substrate includes graphics controller 20 connecting to north bridge device 14. It is recognizable by one of ordinary skill in the art that most computer substrate has video controller built in. It's called video on board. This feature is used to eliminate external video card on a motherboard, for example.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to easily recognize the feature of adding more devices on board such video chip in order to eliminate external devices.

Melo further discloses that a co-processor external 12 (fig. 1).

In regard to claim 13, see above discussion regarding to claim 5.

In regard to claim 14, see above discussion regarding to claim 7.

In regard to claim 15, see above discussion regarding to claim 8.

In regard to claim 23, Ukarawa discloses all of the claimed limitations except the dimensions of the substrate as claimed in claim 23.

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the dimensions because applicant has not disclosed that these dimensions provide an advantage, is used for a particular purpose, or solve a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with either shape because they perform the same function of positioning the module to the substrate.

Therefore, it would have been obvious to one of ordinary skill in the art to modify Ukarawa to obtain the invention as specify in the above claims.

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Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Response to Arguments

7. Applicant's arguments filed 5/9/05 have been fully considered but they are not persuasive. For instance, Applicants contend that the cited reference does not disclose "a standard dimension substrate". It is not clear what a standard dimension substrate is since there was no detail descriptions of the substrate in the specification. Therefore, the "standard dimension" is found to be vague and broad. The cited art in fact discloses a substrate which is capable of carrying semiconductor devices, for example, memory, logic chips, etc.

Applicants further submit that the cited reference does not disclose a router IC. As described by the Applicants, the router is an integrated circuit which is capable of receiving and routing data between multiple locations. The logic chip is indeed an IC device which receives data and distributes data to other devices such as system memory. For example, fig. 19 of Urakawa shows the logic chip receiving data from a DRAM and distributing these data to the memory chips.

Conclusion

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Nathan Ha July 13, 2005

> HOAI V. PHAM PRIMARY EXAMINER